Recipe for Si mask etching (pattern on backside)

4 inch wafer P-type <100>, silicon mask nitride, anisotropic etching (angle 54.74°)

1. LPCVD grow Si_3N_4 300 nm.

2. Silicon nitride patterning by photolithography.
   A. Resist coating on backside (with primer).
      - HMDS. 40 sec at 2000 rpm.
      - AZ1470 pure. 5 sec at 500 rpm. 55 sec at 2000 rpm.

   B. Bake at 90°C for 30 min.
   C. Exposure 9 sec.
   D. Developing 105 sec, developer: H_20 = 1: 2
   E. Post-bake at 120°C for 30 min.

3. Si_3N_4 plasma etching, using CHF_3 and O_2
   Recipe:
      - Power 100 W (2.41).
      - Pressure 10 mbar (valve auto).
      - V_{bias} 500 (V) (in any case swr as high as possible).
      - CHF_3 flow: 50 sccm.
      - O_2 flow: 4 sccm.

      Si_3N_4 etching rate: 42 nm/min (20 Oct 1990).
      Resist etching rate: 10 nm/min (20 Oct 1990).

4. Remove resist with acetone or stripper.

5. Silicon anisotropic etching with KOH at 80-85°C.
      - KOH solution: 440 g KOH with 1 L DI-water.
      - Optional: adjustment of 1-propanol (boiling point at 90°C) to prevent strong KOH vaporization.
      - Silicon etching rate: 1.125 μm/min.
      - Si_3N_4 etching rate: 35×10^{-3} nm/min.

6. Remove Si_3N_4 with HF 40% (skip this step for SiN_x membranes)

N.B. To prevent the nitride layer from damaging during exposure and plasma-etching (scratches) protection may be necessary.

Note: Adapted for use from http://dsa.dimes.tudelft.nl/usage/process_data/SiNx_membranes.html